AN2528
Application note

Very wide input voltage range 6 W SMPS for metering

Introduction

This document presents the design of a universal input power supply for metering applications. The design is mainly based on the following ST parts: an L6565 PWM driver and STC04IE170HP as the main switch. It is linked with the release of the STEVAL-IP001Vxx demo board (see *Figure 1* below). The design is a complete solution for a 5 W single output SMPS, which is widely used as a power supply in metering applications. However the design method can be applied to an SMPS suitable for other applications working on a three-phase mains and it can easily be upgraded for higher output power.

The ESBT base driving circuit as well as guidelines for the optimization of the power dissipation are given.

The influence of parasitic capacitances of the transformer on the ESBT is also explained in detail.

Finally, the most important waveforms and thermal results are given in *Section 5* and *Section 6*. They demonstrate the benefits of using a QR flyback with ESBT.

Refer to AN1889 and AN2254 for the overall design of an auxiliary power supply using ESBT in flyback QR with L6565, while refer to AN2454 for the small signal power switch model with all parasitic components.

Figure 1. STEVAL-ISA030V1

Contents

List of figures

1 Design specifications and schematic diagram

The table below lists the converter specification data and the main parameters fixed for the demo board.

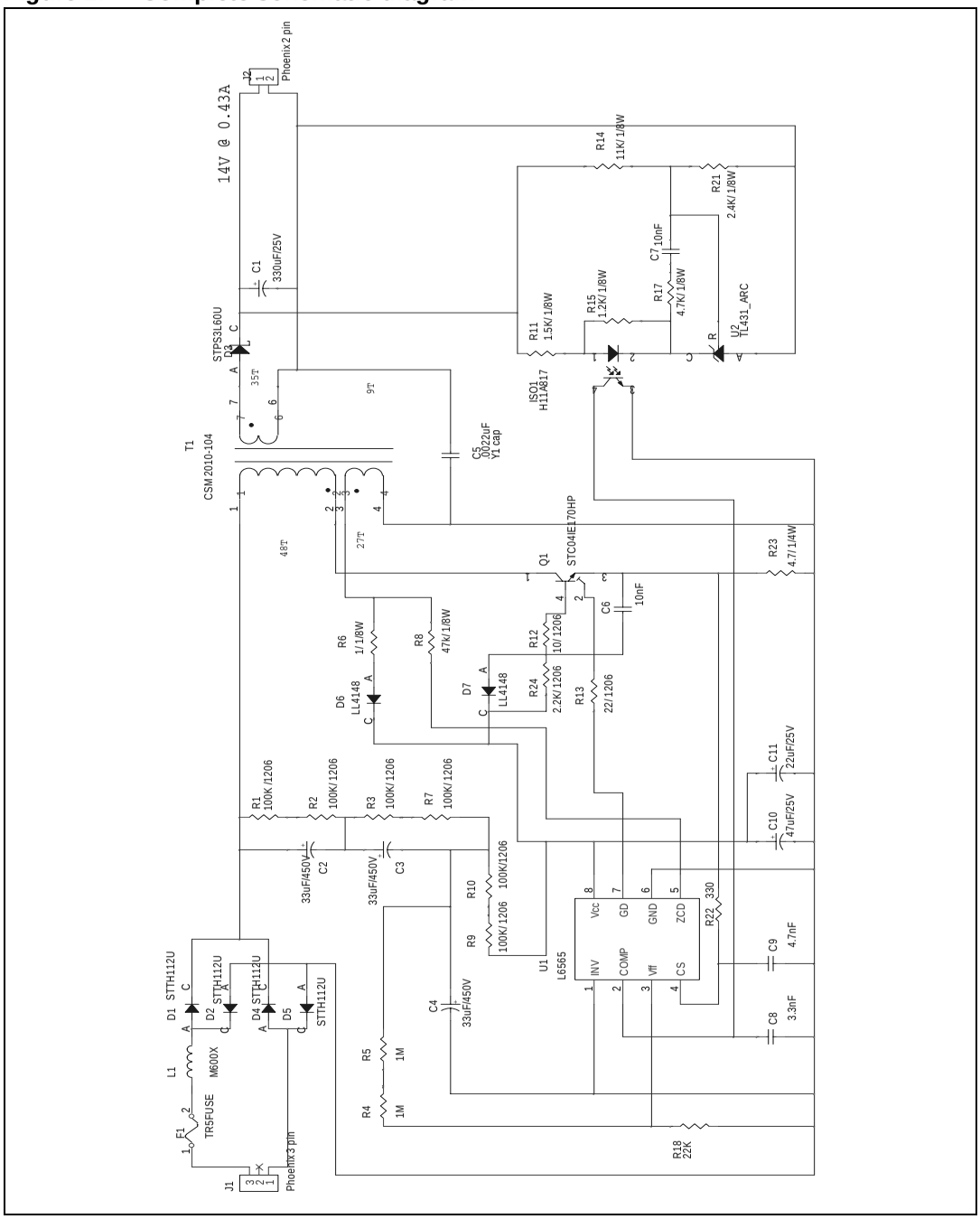
Table 1. Converter specification and preliminary choices

Symbol	Description	Values
V_{inmin}	Rectified minimum input voltage	150
V_{in}	Rectified maximum input voltage	850
V_{out}	Output voltage	14 V/430 mA
P_{out}	Maximum output power	6 W
η	Converter efficiency @ max load	> 80%
F	Minimum switching frequency	$\cong$ 30 kHz
V_{fl}	Reflected flyback voltage	250 V
V_{spike}	Max over voltage limited by clamping circuit	150 V

A schematic diagram of the SMPS is given in *Figure 2*. The most relevant components are:

1. HV ESBT main switch and simple driving circuit
2. L6565 QR PWM driver to get the best efficiency
3. Special transformer construction with very low parasitic capacitance

Figure 2. Complete schematic diagram



2 Flyback stage design

Well known to all SMPS designers, the voltage stress on the device (power switch) is given by:

Equation 1

$$V_{off} = V_{inmax} - V_{fl} - V_{spike}$$

where V_{fl} = flyback voltage = (V_{out} + $V_{F, diode}$) * N_p/N_s and V_{spike} is the over-voltage on the collector due caused by leakage inductance. This over-voltage is not limited by any clamping network in order to minimize as much as possible the solution cost using also the very large margin available which has been fixed to 200 V. N_p is the number of turns on the primary side while Ns is the number of turns on the main output secondary winding.

Now, taking into account a 300 V margin, the maximum flyback voltage that can be chosen is:

Equation 2

$$V_{fl} = BV - V_{inmax} - V_{spike} - V_{margin} = 1700 - 850 - 200 - 300 = 350V$$

After the calculation of the flyback voltage, we can proceed with the next step in the converter design. The turns ratio between primary and secondary side is calculated with the following formula:

Equation 3

$$\frac{N_p}{N_s} = \frac{V_{fl}}{V_{out} + V_{F, diode}} = \frac{350}{14 + 1} = 23.3$$

As a first approximation, since the turn-on of the device occurs immediately after the energy stored on the primary side, inductance is completely transferred to the secondary side:

Equation 4

$$V_{dcmin} \bullet T_{onmax} = V_{fl} \bullet T_{reset}$$

and

Equation 5

$$T_{onmax} - T_{reset} = T_S$$

Where T_{onmax} is the maximum on time, T_{reset} is the time needed to demagnetize the transformer inductance and T_S is the switching time. Combining the two previous formulas T_{onmax} results in:

Equation 6

$$T_{onmax} = \frac{V_{fl} \bullet T_S}{V_{dcmin} + V_{fl}} \cong 14\mu s$$

The next step is to calculate the peak current. The output power is set to 6 W and the desired transformer efficiency must be set by the designer (at least 80% in this case). Excluding the energy losses on the input diode bridge, on the power switch and on the secondary side rectifier, the following approximate formula can be used:

Equation 7

$$P_{IN} = 1.25 \bullet P_{OUT} = \frac{\frac{1}{2} \bullet L_P \bullet I^2_P}{T_s} = \frac{\frac{1}{2} \bullet V^2_{dcmin} \bullet T^2_{onmax}}{L_P \bullet T_S}$$

Hence

Equation 8

$$L_P = \frac{V^2_{dcmin} \bullet T^2_{onmax}}{2.5 \bullet T_S \bullet P_{OUT}} = 14.7mH$$

From here we can now calculate the peak current on primary.

Equation 9

$$I_P = \frac{V_{dcmin} \bullet T_{onmax}}{L_P} \approx 143mA$$

To keep the transformer size very small and to get a very effective cost solution, we prefer to slightly increase the minimum working frequency in order to decrease the primary inductance.

In order to have a 15 mH inductance and to keep an EF20 core, a lot of turns are needed on the primary side. This can generate either not enough space on the EF20 core to accomodate such a high number of windings or the remaining space is not large enough to ensure good design. These considerations might induce designing a smaller primary inductance value accepting a higher switching frequency.

There is no contraindication in using a smaller primary inductance which leads to a higher minimum switching frequency and theoretically also to a higher maximum frequency. However the maximum switching frequency is then limited not only by the inductance value, but also by the L6565 PWM driver. When using an L6565, the internal blanking time limits the minimum off-time and, in turn, the maximum switching frequency. To better understand this phenomenon, please refer to the L6565 datasheet and to the next paragraphs.

After bench tests and fine tuning we used a transformer with the following specs:

Equation 10

$$L_P = 7.5mH$$

Equation 11

$$\frac{N_p}{N_s} = 23.8 \qquad \frac{N_p}{N_{aux}} = 18.87$$

The part number of the transformer is CSM 2010-104 from Cramer.

In the next *Section 3*, we see from bench verification that the real minimum working frequency is 50 kHz even if the inductance is 7.5 mH but with a peak current of about 250 mA.

3 Parasitic capacitances and related issues

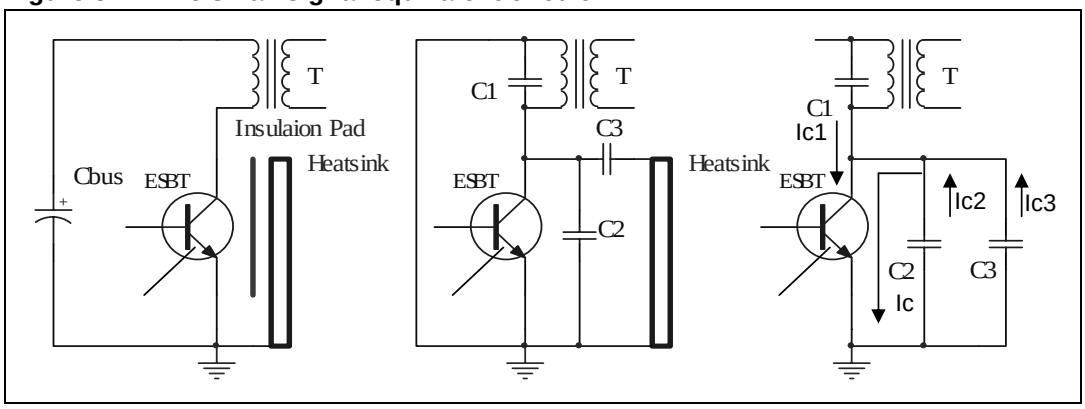
In a flyback converter stage it is important to take into account the parasitic capacitances since their influence may affect the correct operation of the converter itself. *Figure 2* shows the small signal equivalent model of a main switch, transformer and main parasitic effects.

The parasitic capacitances between the ESBT collector and ground are mainly due to three components (see *Figure 2*):

1. C_1, the primary inter-winding capacitance;
2. C_2, the intrinsic capacitance of ESBT between its collector and source;
3. C_3, the parasitic capacitance between the collector of the ESBT and the heat-sink.

Usually transistors are mounted on a heat-sink by interposing an insulation layer. The heat-sink has to be grounded either for safety reasons, or to minimize the RFI. The resulting total parasitic capacitance C is equal to $C_1 + C_2 + C_3$. C may be large enough to produce additional and non-negligible switch-on power dissipation. Large parasitic capacitances may cause ringing and produce noise problems. The effect of parasitic capacitances is worse at higher input voltages, like those observed in a 3-phase power supply.

Figure 3. The small signal equivalent circuit



Considering that the power managed by the system is low, another goal to achieve is to keep the power dissipation very low on every part on the system. Our target is to get less than 1.5 W power loss on the switch. Achieving this target leads to two benefits: high efficiency and no need of heat-sink (cost reduction).

Therefore the effect of C_3 must not be considered in this case. C_2 is related only to additional power dissipation during switch-on and does not affect system stability. C_1 has the most important effect on flyback converter design. We have only two ways to reduce C_1:

1. Parasitic transformer inter-winding capacitance
2. Layout parasitic capacitance

Care is needed when designing the layout and building the transformer.

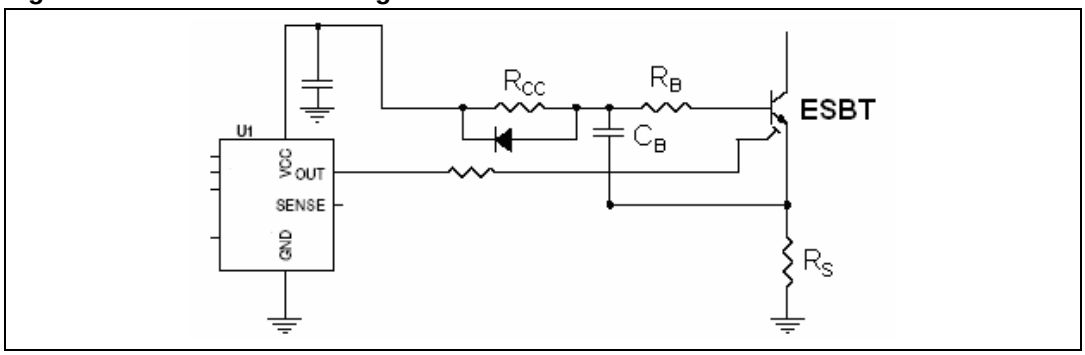
4 Base drive circuit design

Let's have a closer look at the very simple base drive network used in this application. Normally in applications such SMPS, where the load is variable, the collector current varies as well. It is very important to provide a base current to the device that is correlated with the collector current in order to avoid the over saturation of the device at low load and to optimize its performance in terms of power dissipation. This implies the use of a driving network which allows getting a base current proportional to the collector current. For additional information about the ESBT proportional base driving method, refer to AN2131.

Since in our application we must take into account power dissipation and simplicity as well, we have preferred the simplest and least expensive driving network which is shown in *Figure 4*. This choice also satisfies power dissipation requirements.

To set the R_{CC} value some considerations must be done. First of all, refer to the h_{FE} curve of STC04IE170HP (*Figure 5*).

Figure 4. ESBT base driving network



Referring to the calculations in *Section 2*, the collector peak current is 250 mA. At this current value the ESBT gain is about 20, so that theoretically just 250 / 20 = 12.5 mA should be enough to drive the base. This is true for very long conduction time. In the present example the dynamic phenomenon can occur due to the relatively high switching frequency (higher than 50 kHz) and even more to the small conduction time.

This concept is illustrated in *Figure 6*. It is extracted from the STC04IE170HP datasheet and shows that, right after the turn-on, the V_{CS} needs some time to reach the V_{CSSAT} value. This time is proportional to the collector current amount. That is why a peak base current is absolutely mandatory to have a low voltage drop during conduction as soon as possible.

For further details about the driving network, please refer to AN2454.

Figure 5. DC current gain

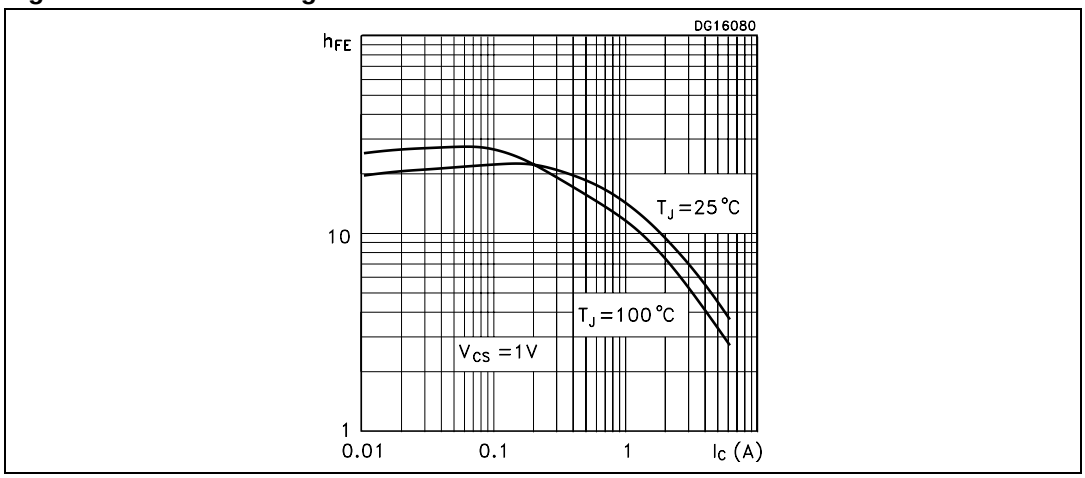
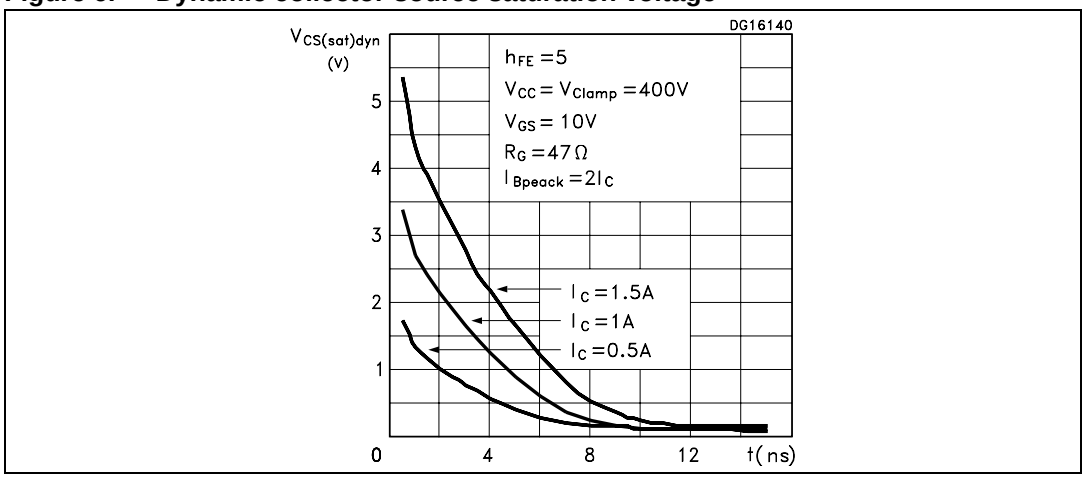


Figure 6. Dynamic collector-source saturation voltage



To maximize performances, a base capacitor C_B has been inserted.

Note that, using the driving network shown in *Figure 4*, a quasi total recovery of energy to drive the base is achieved. During the storage time the collector current comes out from the base and is stored in the base capacitor. If the capacitor is small enough, the voltage across it reaches the V_{cc} and after that the current flows to the V_{cc} capacitor.

To set the time duration of the base current spike, the following approximate formula is useful:

Equation 12

$$t_{peak} = 3 \bullet R_B \bullet C_B$$

Since R_B=10 Ω (see below), if the peak has to be about 300 ns

Equation 13

$$C_B = \frac{t_{peak}}{3 \bullet R_B} = 10nF$$

The aim of R_B is to dampen the ringing on the base current at the end of its peak. It is chosen as a compromise between a damping effect and additional power dissipation on it.

Ten is big enough to remove any ringing and the additional power dissipation on it is practically negligible due to the very low current flowing through it. Finally, knowing that V_{cc} is about 15 V:

Equation 14

$$R_{CC} = \frac{15V}{12.5mA} = 1.2K\Omega$$

After bench verification a final R_{CC} of 2.2 kΩ has been fixed. A smaller base current than the forecasted one flows into the base (higher I_C/I_B ratio) compensated by a higher base current during the peak (much lower I_C/I_B ratio for a very short time).

5 Experimental results: waveforms

The following figures show the main waveforms in steady state condition at full load. Notice the behavior of the base current with an initial high peak pulse needed to minimize the effect of the dynamic saturation voltage.

Figure 7. 110 V_{ac} input voltage overall1

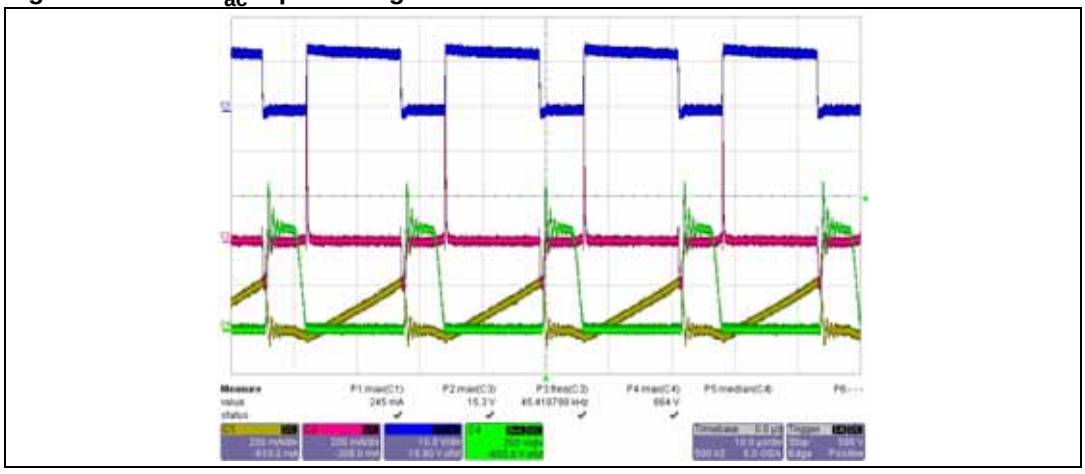


Figure 8. 110 V_{ac} input voltage overall2

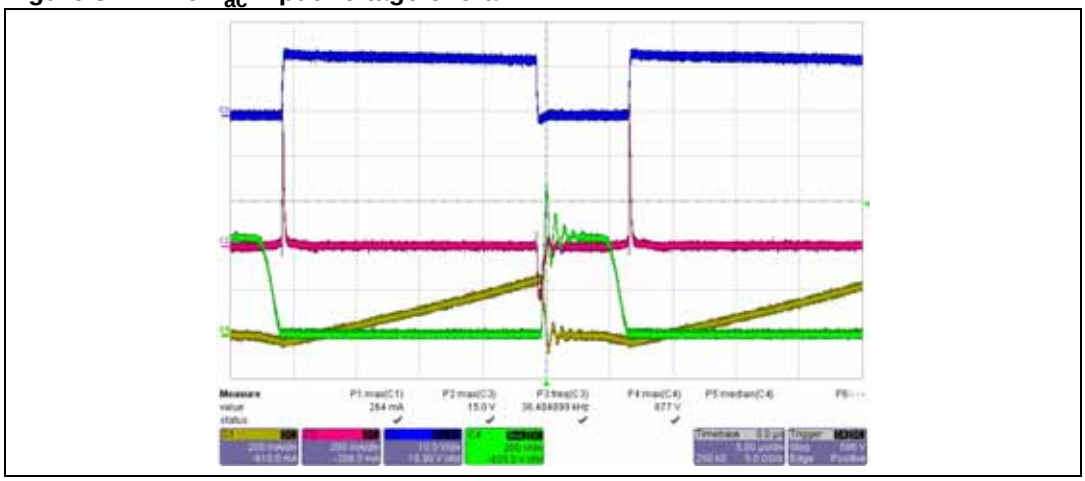


Figure 9. 110 V_{ac} input voltage- storage highlight

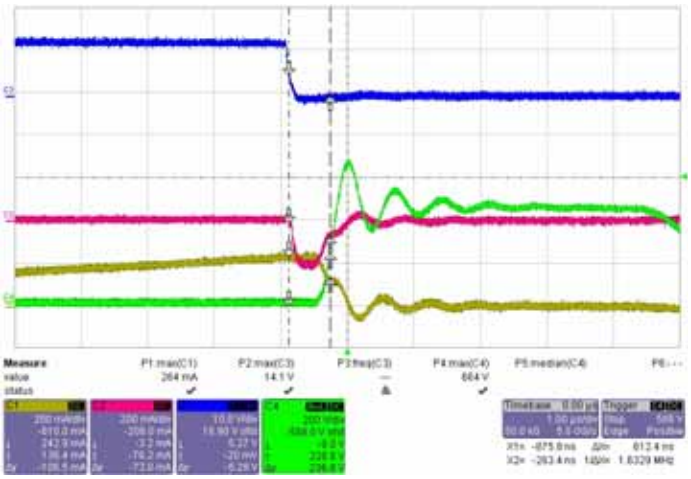


Figure 10. 110 V_{ac} input voltage turn-off highlight

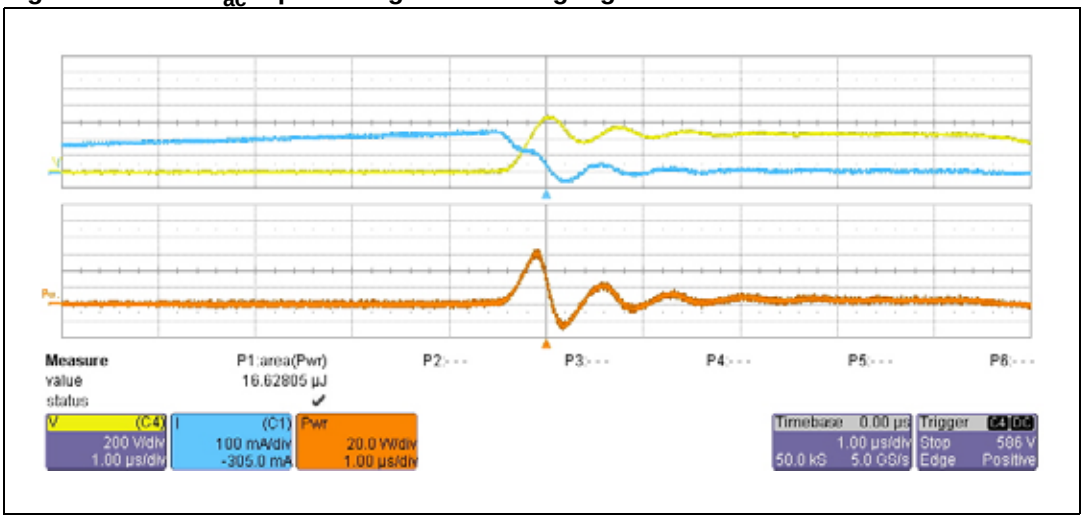


Figure 11. 380 V_{ac} input voltage overall1

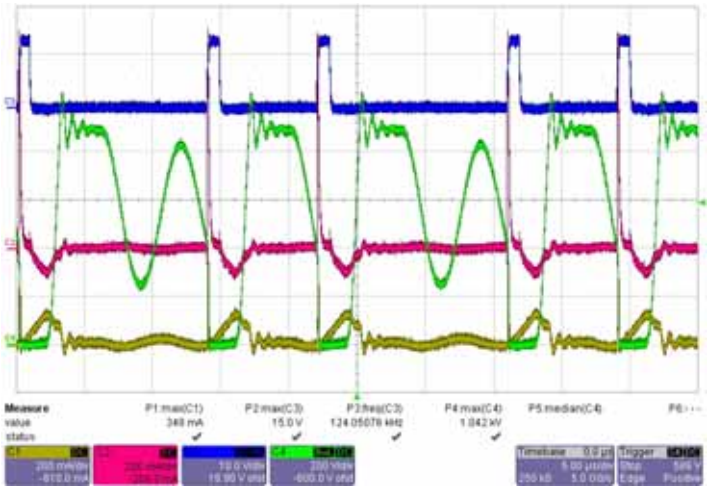


Figure 12. 380 V_{ac} input voltage overall2

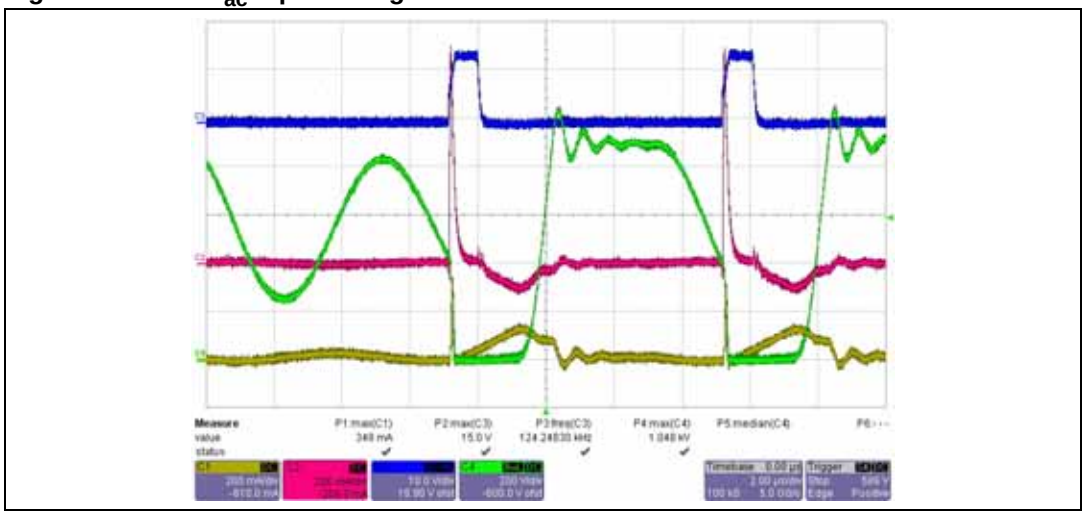


Figure 13. 380 V_{ac} input voltage storage time highlight

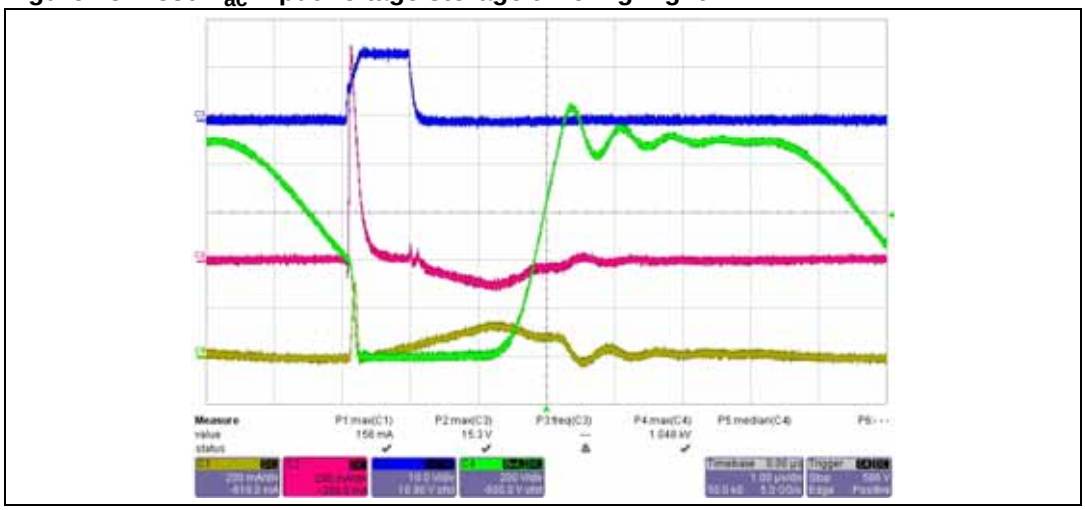


Figure 14. 380 V_{ac} input voltage - turn-on highlight

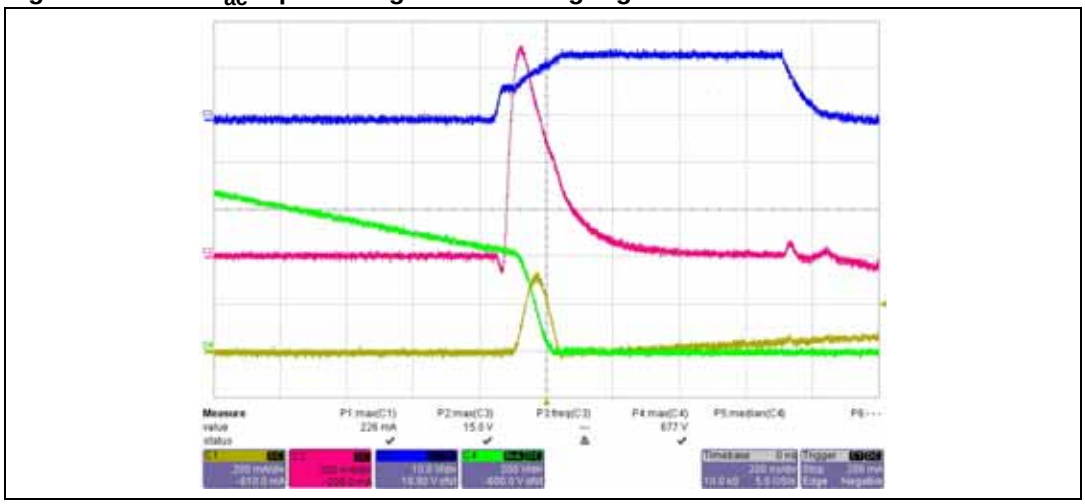


Figure 15. 600 V_{ac} input voltage overall1

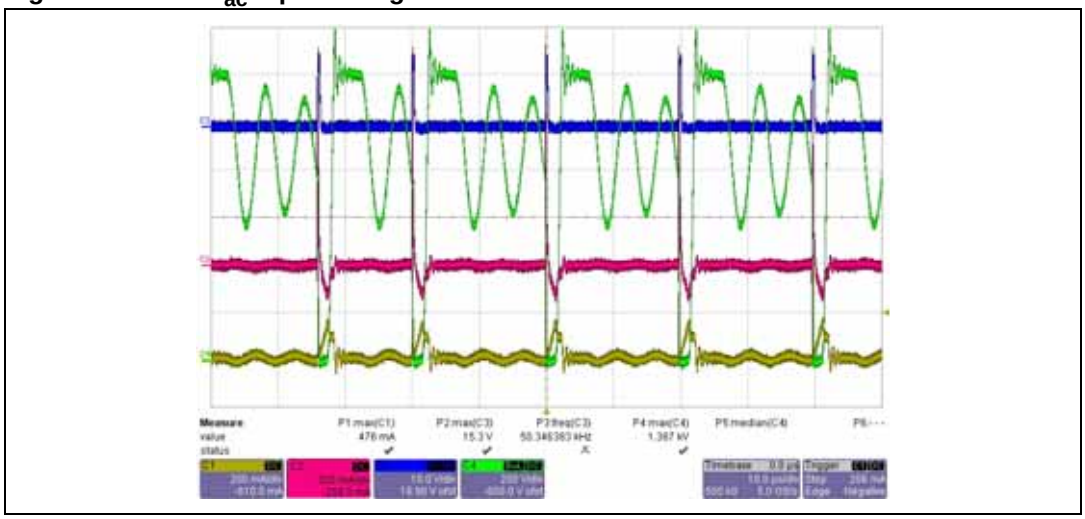


Figure 16. 600 V_{ac} input voltage overall2

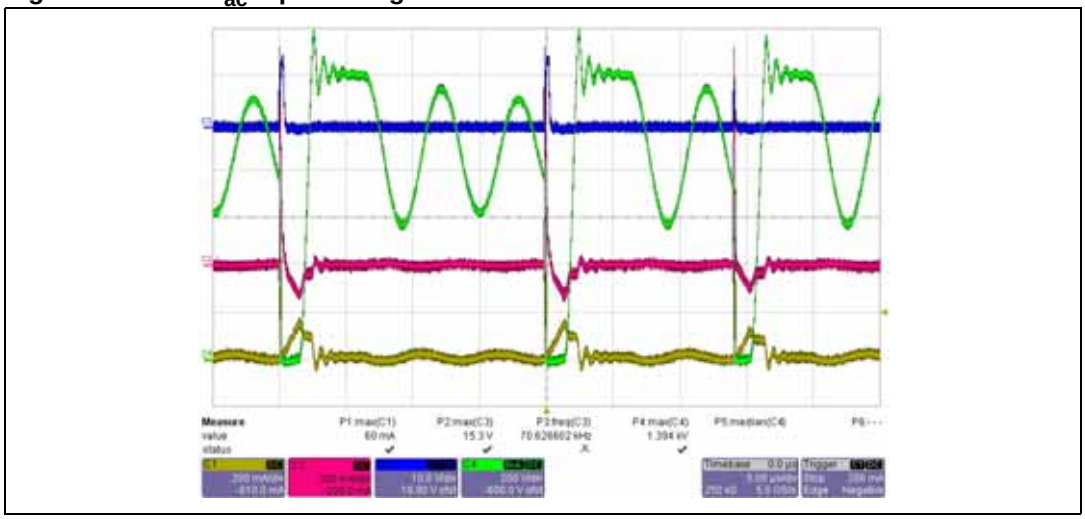


Figure 17. 600 V_{ac} input voltage turn-off highlight

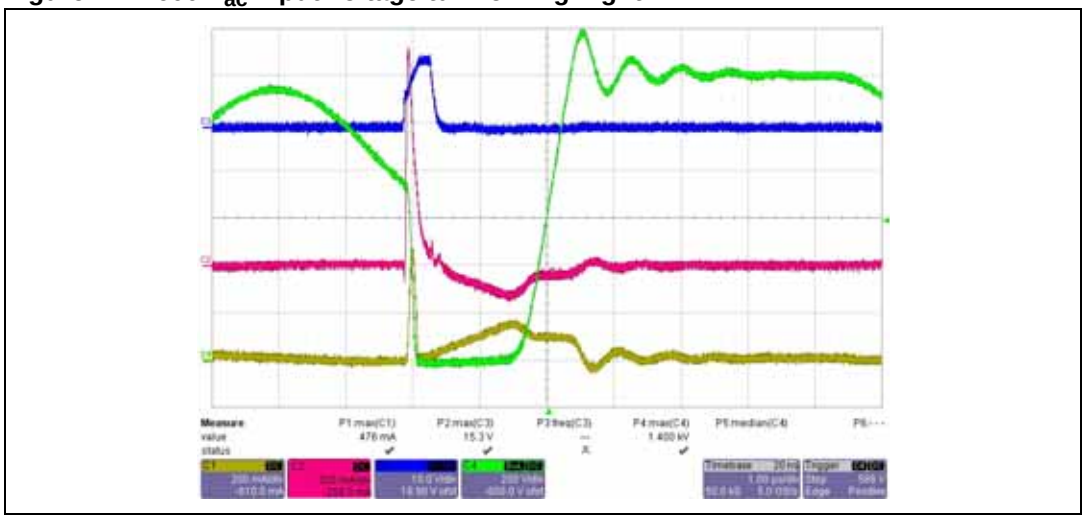
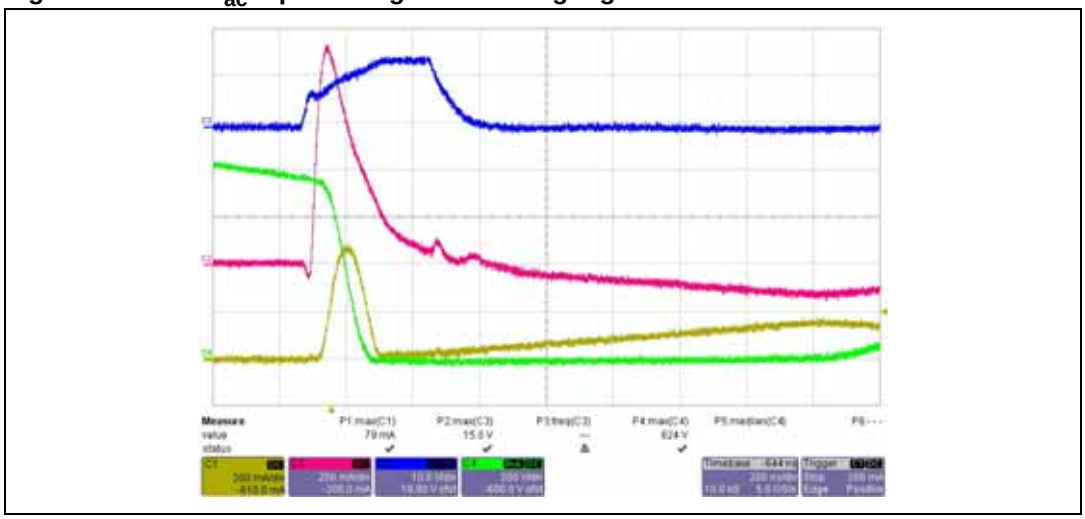


Figure 18. 600 V_{ac} input voltage turn-on highlight



The importance of having a very good transformer in the turn-on highlight at high input voltage can be better observed. The collector current leading edge at turn-on is evident in this condition. The peak amplitude has to be controlled or it can lead to premature turn-off of the PWM driver with consequent instability. This issue has been deeply discussed in *Section 3*.

6 Experimental results: efficiency and further considerations

Table 2 summarizes the thermal and loss data. All information refers to max load. An excellent result is the very high efficiency also at the highest input voltage. The case temperature of ESBT is fine even in the worst case, with consequent low power dissipation on it.

Table 2. Power dissipation and efficiency

VinAC (V)	Tc (°C)	Ptot (W)	Efficiency
110 (V)	34	0.3	80%
400 (V)	49	0.8	66%
600 (V)	73	1.6	55%

To get the thermal performances shown, a special feature of the bipolar has been positively utilized.

In a standard QR mode of operation, when the input voltage rises higher and higher, the switching losses should increase since the frequency is increasing. For this reason the L6565 provides the frequency foldback function that limits the minimum OFF-time.

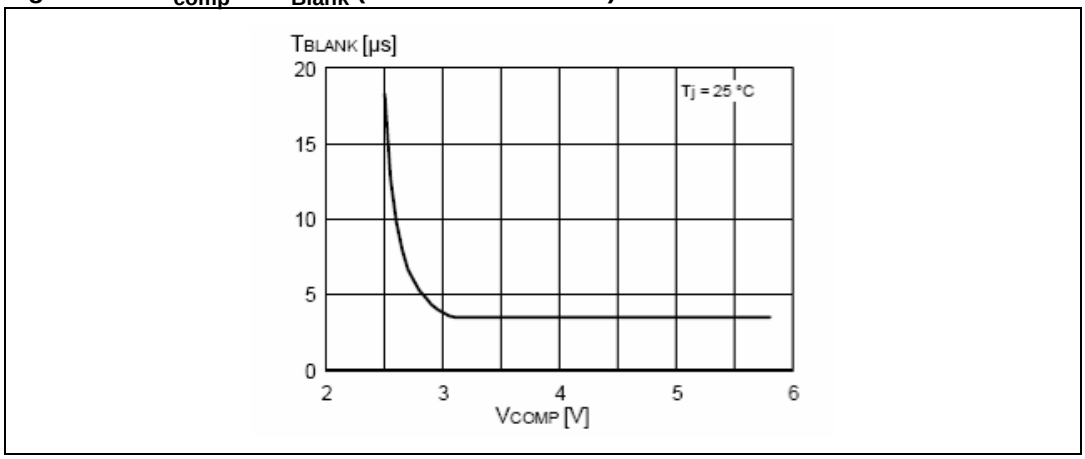
An added feature is given by the storage time of ESBT, that helps to further reduce the frequency while increasing the Input Voltage and/or reducing the load. This frequency

reduction at high input voltage is very effective in improving the overall efficiency, since the higher turn-on and turn-off voltages make the switching losses critical.

Thanks to the storage time (lasting about 1.5 µs under this condition), that adds a delay to the current on-time, the minimum on-time is much longer than the one imposed by the L6565.

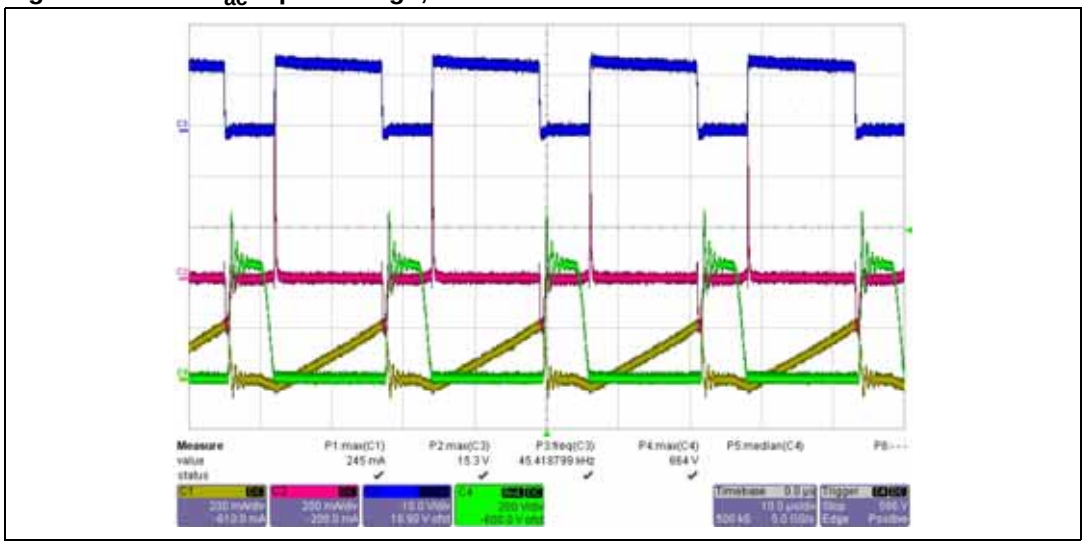
This leads to a lower V_{comp} value, and as a consequence, to a longer minimum OFF-time (see *Figure 19* below). The system then works in advance at lower frequency as soon as the input voltage increases or the load decreases.

Figure 19. V_{comp} vs T_{Blank} (minimum OFF-time)



In the next figures the frequency reduction as a consequence of an increased input voltage is shown.

Figure 20. 110 V_{ac} input voltage, max load



From *Figure 21* the frequency is reduced due to the storage time presence at 380 V_{ac}, becoming more and more evident at higher input voltage, 600 V_{ac}.

This "enhanced" frequency foldback created by the storage time allows keeping the total power dissipation on the device very low regardless of the very high voltage needed to sustain.

Figure 21. 380 V_{ac} input, max load: frequency reduction

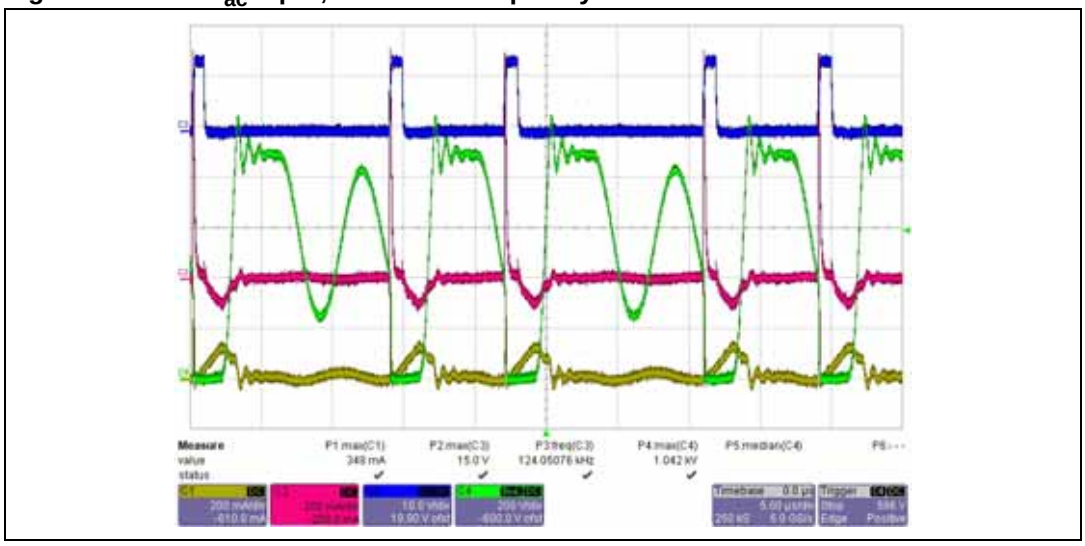


Figure 22. 600 V_{ac} input, max load: further frequency reduction

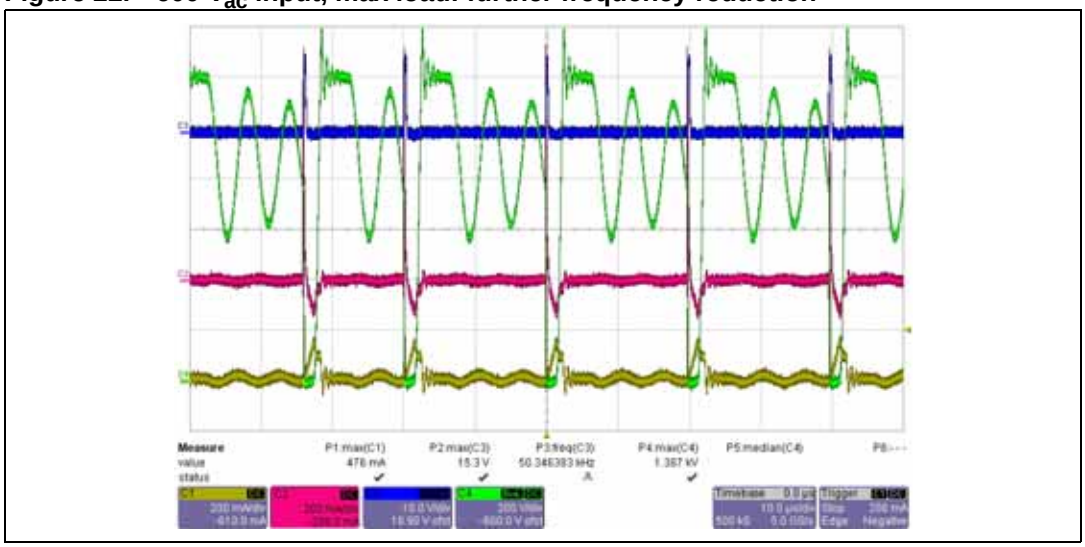
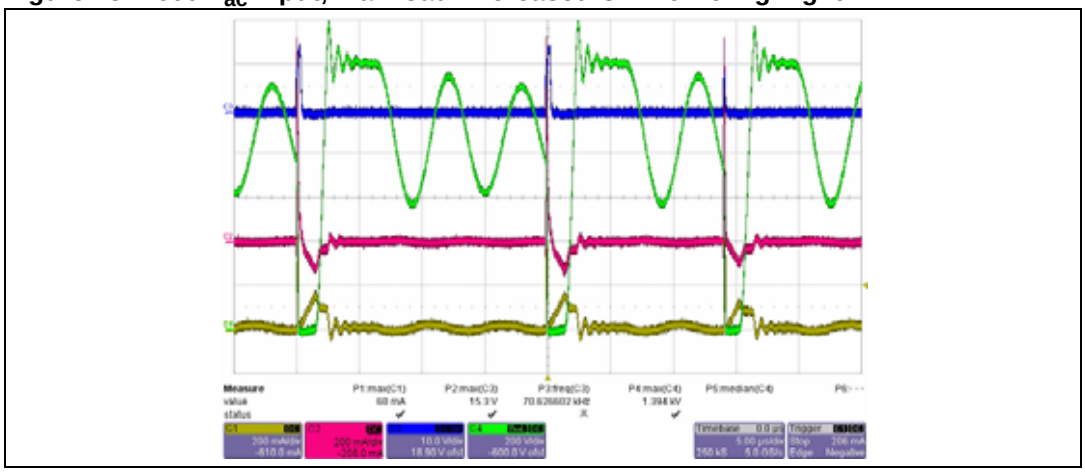


Figure 23. 600 V_{ac} input, max load: increased OFF- time highlight



Appendix A Bill of materials

Table 3. Bill of materials

Reference	Qty	Value/part number	Description
C1	1	330 µF / 25V	Electrolytic capacitor
C2, C3, C4	3	33 µF / 450V	Electrolytic capacitor
C5	1	.0022 µF	ceramic capacitor, 440 V_{ac}, 2 KV
C6, C7	2	10 nF / 50 V	ceramic capacitor, 50 V, X7R
C8	1	3.3 nF / 50 V	ceramic capacitor, 50 V, X7R
C9	1	4.7 nF / 50 V	ceramic capacitor, 50 V, X7R
C10	1	47 µF / 25 V	Electrolytic capacitor
C11	1	22 µF / 25 V	Electrolytic capacitor
D1, D2, D4, D5	4	STTH112U	STMicroelectronics, diode rectifier, 1200 V, 1 A
D3	1	STPS3L60	STMicroelectronics, diode power schottky, 60 V, 3 A
D6, D7	2	LL4148	SMD 1206
F1	1	TR5Fuse	Serie TR5 250 mA / 250 V
ISO1	1	H11A817	Phototransistor Optocouplers, Fairchild
J1	1	Phoenix 3 pin	
J2	1	Phoenix 2 pin	
L1	1	M600X	Radiali, 470 µH
Q1	1	STC04IE170HP	STMicroelectronics, emitter switched Bipolar transistor, 4 A, 1700 V
R1, R2, R3, R7, R9, R10	6	100 K	SMD 1206
R4, R5	2	1 M	SMD 1206
R6	1	1	SMD 1206
R8	1	47 K	SMD 1206
R11	1	1.5 K	SMD 1206
R12	1	10	SMD 1206
R13	1	22	SMD 1206
R14	1	11 K	SMD 1206
R15	1	1.2 K	SMD 1206
R17	1	4.7 K	SMD 1206
R18	1	22 K	SMD 1206
R21	1	2.4 K	SMD 1206
R22	1	330	SMD 1206
R23	1	4.7 / 1/2 W	Resistor, carbon film, 350 V, 0.5 W, 5%

Table 3. Bill of materials (continued)

Reference	Qty	Value/part number	Description
T1	1	CSM 2010-104	CRAMER [sample]
U1	1	L6565	STMicroelectronics, Q-resonant SMPS controller
U2	1	TL431C	STMicroelectronics, Shunt Reference, 2,5 V, 1 to 100 mA

Appendix B PCB layout

Figure 24. PCB picture top view (components and copper)

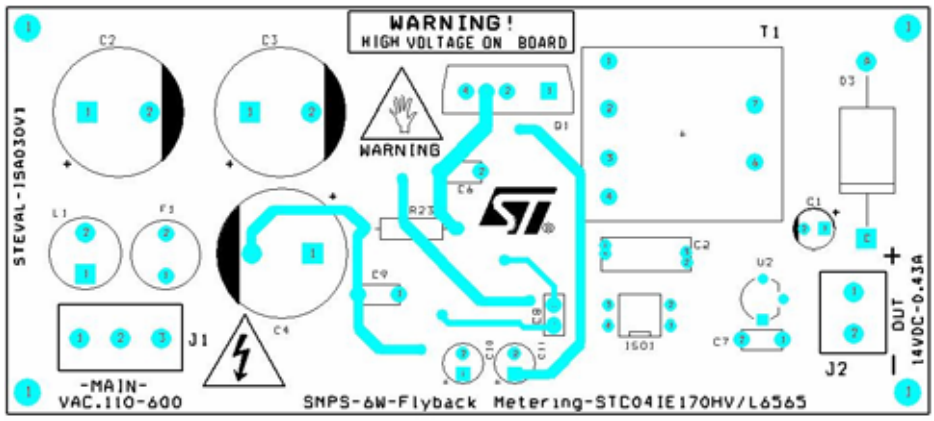


Figure 25. PCB picture top view components and bottom layer copper

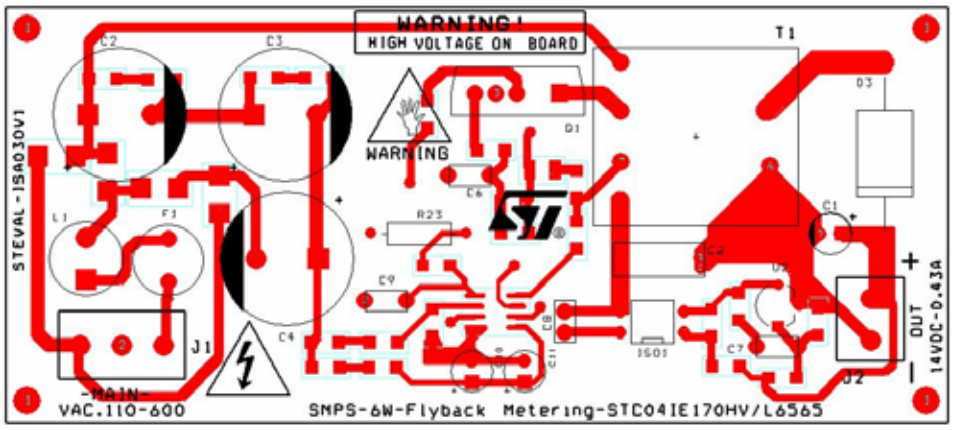
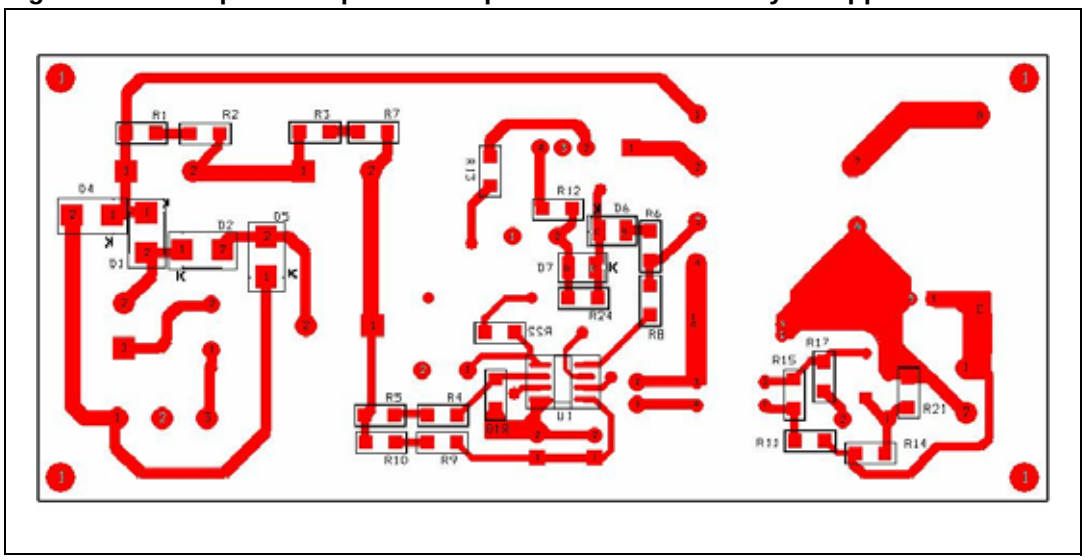


Figure 26. PCB picture top view components and bottom layer copper



7 References

- STMicroelectronics application note AN1889 "ESBT STC03DE120 IN 3-PHASE AUXILIARY POWER SUPPLY"
- STMicroelectronics application note AN1262 "OFFLINE FLYBACK CONVERTERS DESIGN METHODOLOGY WITH THE L6590 FAMILY"
- STMicroelectronics application note AN2131 "HIGH POWER 3-PHASE AUXILIARY POWER SUPPLY DESIGN BASED ON L5991 AND ESBT STC08DE150"
- STMicroelectronics L6565 datasheet
- STMicroelectronics STC04IE170HV datasheet
- "Switching Power Supply Design", McGraw-Hill, Inc.

8 Revision history

Table 4. Revision history

Date	Revision	Changes
05-Jul-2007	1	First issue